IN THE CLAIMS

1. (Currently Amended) An image processor comprising:

a storage circuit storing therein image data;

a data input/output circuit controlling input/output of the image data;

an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit;

a refresh circuit controlling refreshing of said storage circuit; and

a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out,

said memory control circuit comprising ~~an area~~ a window adjustment circuit which sets up an additional [[area]] window adjacent to ~~an area~~ a window in which the image data are actually stored in a memory space of said storage circuit and storing therein additional data other than the image data, which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the additional data in the additional [[area]] window, in response to the address and a read control signal supplied to said storage circuit,

wherein the additional data are written in with an address of the additional [[area]] window.

2. (Currently Amended) The image processor in accordance with claim 1, wherein said [[area]] window adjustment circuit sets up the additional [[area]] window immediately preceding or following the [[area]] window in which the image data is stored.

3. (Currently Amended) The image processor in accordance with claim 1, wherein information on a position of the additional [[area]] window is supplied as setting information included in header information.

4. (Currently Amended) The image processor in accordance with claim 2, wherein said [[area]] window adjustment circuit sets a size of the additional [[area]] window using information, which is obtained in synchronization with a supplied vertical synchronization signal, as a parameter and reads out the data stored in the additional [[area]] window in response to a data transfer request.

5. (Currently Amended) The image processor in accordance with claim 1, wherein said [[area]] window adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter.

6. (Currently Amended) The image processor in accordance with claim 2, wherein said [[area]] window adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter.

7. (Currently Amended) The image processor in accordance with claim 4, wherein said [[area]] window adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter.

8. (Currently Amended) The image processor in accordance with claim 5, wherein said [[area]] window adjustment circuit supplies the additional data, which is

read out from the additional [[area]] window, to a predetermined position in a video signal.

9. (Currently Amended) The image processor in accordance with claim 6, wherein said [[area]] window adjustment circuit supplies the additional data, which is read out from the additional [[area]] window, to a predetermined position in a video signal.

10. (Currently Amended) The image processor in accordance with claim 7, wherein said [[area]] window adjustment circuit supplies the additional data, which is read out from the additional [[area]] window, to a predetermined position in a video signal.

11. (Previously Presented) The image processor in accordance with claim 1, wherein said access control circuit supplies the additional data other than the image data to said memory circuit.

12. (Currently Amended) An image processing method comprising the steps of:

setting up, in a storage circuit in which image data is stored, a range of an image [[area]] window in which the image data is written and a range of an additional [[area]] window which is adjacent to the image [[area]] window and in which data other than the image data is written, with information supplied to a memory space of said storage circuit as a parameter;

writing the additional data other than the image data from external into the additional [[area]] window in said storage circuit according to a first write control signal;

writing the image data at an address location of the image [[area]] window in said storage circuit according to a second write control signal; and

reading out the additional data stored in the additional [[area]] window and the image data stored in the image [[area]] window in said storage circuit in response to a first read control signal,

wherein the additional data are written in with an address of the additional [[area]] window.

13. (Currently Amended) The image processing method in accordance with claim 12, wherein said step of reading out the additional data comprises the steps of:

reading out the additional data from the additional [[area]] window in said storage circuit in response to the first read control signal; and

reading out the image data from the image [[area]] window in said storage circuit in response to a second read control signal.

14. (Original) The image processing method in accordance with claim 12, wherein the first write control signal and the read control signal are a transfer enable signal enabling an execution of processing.

15. (Currently Amended) The image processing method in accordance with claim 12, wherein said step of reading out the additional data inserts the additional data read out from the additional [[area]] window into a predetermined position of a video signal.

16. (Currently Amended) An image processor comprising:

a storage circuit storing therein image data;

a data input/output circuit controlling input/output of the image data;

an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit;

a refresh circuit controlling refreshing of said storage circuit; and

a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out, and generating an additional address of a width same as the address in said storage circuit to and from which data other than the image data is written in and read out,

said memory control circuit comprising ~~an area~~ a window adjustment circuit which sets up an additional [[area]] window corresponding to the additional address and which is adjacent to ~~an area~~ a window in which the image data are actually stored in a memory space of said storage circuit and storing therein data other than the image data, which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the additional data in the additional [[area]] window, in response to the address and a read control signal supplied to said storage circuit, wherein the additional data are written in with an address of the additional [[area]] window.

17. (Currently Amended) An image processing method comprising the steps of:

setting up, in a storage circuit in which image data is stored, an address space for a range of an image [[area]] window in which the image data is written, and an additional address space of a width same as the address space for a range of an additional [[area]] window which is adjacent to the image [[area]] window and in which data other than the image data is written, with information supplied to a memory space of said storage circuit as a parameter;

writing the additional data other than the image data from external into the additional [[area]] window in said storage circuit according to a first write control signal;

writing the image data at an address location of the image [[area]] window in said storage circuit according to a second write control signal; and

reading out the additional data stored in the additional [[area]] window and the image data stored in the image [[area]] window in said storage circuit in response to a first read control signal, wherein the additional data are written in with an address of the additional [[area]] window.

18. (Currently Amended) The image processor in accordance with claim 1, wherein said additional [[area]] window has an adjustable width.

19. (Currently Amended) The image processor in accordance with claim 16, wherein said additional [[area]] window has an adjustable width.

20. (Currently Amended) The image processing method in accordance with claim 17, wherein said additional [[area]] window has an adjustable width.

21. (Currently Amended) An image processing method comprising the steps of:

setting up, in a storage circuit in which image data is stored, a range of an image [[area]] window in which the image data is written and a range of an additional [[area]] window which is adjacent to the image [[area]] window and in which data other than the image data is written, with information supplied to a memory space of said storage circuit as a parameter;

writing the additional data other than the image data from external into the additional [[area]] window in said storage circuit according to a first write control signal;

writing the image data at an address location of the image [[area]] window in said storage circuit according to a second write control signal; and

reading out the additional data stored in the additional [[area]] window and the image data stored in the image [[area]] window in said storage circuit in response to a first read control signal,

wherein the additional data are written in with an address of the additional [[area]] window; and

wherein the additional data are teletext data.